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Abatchev et al.

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(54) **METHODS FOR INTEGRATED CIRCUIT FABRICATION WITH PROTECTIVE COATING FOR PLANARIZATION**

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CPC H01L 21/0337; H01L 21/31144; H01L 21/306; H01L 21/30625; H01L 21/31051; H01L 21/31111; H01L 21/31055
See application file for complete search history.

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(57) **ABSTRACT**

Various pattern transfer and etching steps can be used to create features. Conventional photolithography steps can be used in combination with pitch-reduction techniques to form superimposed, pitch-reduced patterns of crossing elongate features that can be consolidated into a single layer. Planarizing techniques using a filler layer and a protective layer are disclosed. Portions of an integrated circuit having different heights can be etched to a common plane.

10 Claims, 46 Drawing Sheets